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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/413,177	10/07/1999	LAP CHAN	CS99-107	1672

28112 7590 01/09/2003

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 01/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/413,177

Applicant(s)

CHAN ET AL.

Examiner

Paul E Brock II

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 19-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 October 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election with traverse of Group I, claims 1 – 18 in Paper No. 5 is acknowledged. The traversal is on the ground(s) that the method claims necessarily use the product and vice versa, and therefore require the same search. This is not found persuasive because it has been shown that a materially different process than that which is claimed can make the product.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 19 – 21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 5.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 – 18 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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With regard to claim 1, it is not clear in claim 1 if “patterning a first layer of oxide” is the same as “forming a first and a second opening through said first layer of oxide.” Are there two steps defining the first layer of oxide? For purposes of this office action “said forming a structure for a first layer of cavities further comprising forming a first and a second opening through said first layer of oxide” will be considered --said patterning a first layer of oxide further comprising forming a first and a second opening through said first layer of oxide--.

With further regard to claim 1, it is not clear in claim 1 if “patterning a second layer of oxide” is the same as “forming a first and a second opening through said second layer of oxide.” Are there two steps defining the second layer of oxide? For purposes of this office action “said forming a structure for a second layer of cavities further comprising forming a first and a second opening through said second layer of oxide” will be considered --said patterning a second layer of oxide further comprising forming a first and a second opening through said second layer of oxide--.

With regard to claim 2, it is not clear if there are two metal layers defined by “a layer of metal” and “a metal layer”. For purposes of this office action the recitation of “a layer of metal that has” will be considered --said metal layer having--.

It should be noted that repetitive use of “a” after a feature has been defined is misleading. For example, in claim 3, “a first layer of a disposable solid” should be “said first layer of disposable solid.” In fact all cases of “a disposable solid” should be replaced by “disposable solid” for clarity.

It is not clear in claim 3 if “depositing a first layer of disposable solid” and “creating an opening in said first layer of disposable solid” is the same step as “applying and patterning a first

layer of disposable solid.” How many first layers of disposable solid is there? How are they defined? All similar repetitive language in this and other claims is also indefinite.

It is not clear in claim 4 if “depositing a second layer of disposable solid” and “creating an opening in said second layer of disposable solid” is the same step as “applying and patterning a second layer of disposable solid.” How many second layers of disposable solid is there? How are they defined? All similar repetitive language in this and other claims is also indefinite.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 2, 5, 6, 15 – 17, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (USPAT 5413962, Lur) in view of Staudinger et al. (USPAT 5481131, Staudinger).

Lur discloses a method of forming air gaps within an integrated circuit structure in figures 1 – 11.

With regard to claim 1, Lur discloses in figure 1 providing a partially fabricated integrated circuit structure (20, 22 – 24, and 28) and depositing a layer of dielectric (30) thereon. Lur discloses in figure 1 forming a metal layer (40) on the surface of the dielectric layer. Lur discloses in figure 1 depositing a thin layer of oxide (bottom most, 42) over the surface of the

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dielectric layer thereby including the metal layer. Lur discloses in figures 2 – 7 forming a structure for a first layer of cavities over the surface of the thin layer of oxide and aligned with the metal layer the forming a structure for a first layer of cavities comprising applying (bottom most, 34) and patterning (27) a first layer of disposable solid followed by applying (third from bottom, 42) and patterning (processing between figures 6 and 7) a first layer of oxide, the patterning a first layer of oxide further comprising forming a first (between the second and third from left, 51's) and a second (between the fourth and fifth from left, 51's) opening through said first layer of oxide. Lur discloses in figures 9 and 10 forming a structure for a second layer of cavities above and aligned with the structure for the first layer of cavities the forming a structure for a second layer of cavities comprising applying (top most, 34) and patterning (top via defining topmost contact 29) a second layer of disposable solid followed by applying (topmost 42) and patterning (figure 10) a second layer of oxide, the patterning a second layer of oxide further comprising forming a first (space between left most 70's) and a second (space between right most 70's) opening through said second layer of oxide. Lur discloses in figure 11 creating the first (bottom most section of 85) and the second (top most section of 85) layer of cavities. Lur discloses in figure 11 performing an oxide (80) deposition over the surface of the second layer of cavities creating a thin layer of oxide. Lur does not disclose forming a metal inductor on the surface of the thin layer of oxide. Staudinger teaches in figure 2 forming a metal inductor (21) on a surface of a thin layer of oxide (36). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the metal inductor of Staudinger on the thin oxide of Lur in order to optimize the size and weight of the semiconductor device by integrating

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both active and passive components onto the same chip as stated by Staudinger in column 1, lines 12 – 26.

With regard to claim 2, Lur discloses in figure 1 the forming a metal layer on the surface of the dielectric layer is forming the metal layer having the cross section of a square or a rectangle with essentially vertical sides whereby the height of the metal layer is equal to the thickness of a conventional semiconductor metal layer whereby a width of the metal layer is equal to or exceeds its height by a measurable amount.

With regard to claim 5, Lur discloses in figures 10 and 11 that the creating a first and a second layer of cavities is removing the first and second layer of disposable solid, the removal to take place by accessing the first and second layer of disposable solid by means of the first and second openings created in the second layer of oxide furthermore by accessing the first layer of disposable solid by means of the first and second openings in the first layer of oxide.

With regard to claim 6, Lur discloses in figures 10 and 11 that the performing an oxide deposition over the surface of the second layer of cavities is creating a thin layer of oxide over the surface of the second layer of oxide thereby furthermore closing off the first and the second openings created in the second layer of oxide.

With regard to claims 15, Staudinger teaches in figures 13 – 15 that the inductor is spiral shaped.

With regard to claims 16, Staudinger teaches in figures 13 – 15 that the inductor is circular shaped.

With regard to claim 17, Staudinger teaches in figures 13 – 15 the polygonal inductor is an octagon.

With regard to claim 22, Lur discloses in figures 10 and 11 the layers of disposable solid being layers of nitride.

7. Claims 8 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of Havemann et al. (USPAT 5668398, Havemann).

Lur and Staudinger do not teach that the disposable solid comprises a polymer.

With regard to claim 8, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 a disposable solid that comprises a polymer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the polymer of Havemann as the first and second disposable solids of Lur and Staudinger in order to form air gaps between metal leads of a semiconductor device using a class of materials that has a wide range of process flexibility based on material selection and process parameters.

With regard to claim 9, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 the creating cavities is heating the substrate in oxygen, evaporating the disposable solid layer using O<sub>2</sub> plasma.

With regard to claim 10, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 the creating a layer of cavities is introducing a solvent to the substrate dissolving the polymer.

With regard to claim 11, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 wherein creating a first and a second layer of cavities is heating the substrate, evaporating the polymer.



With regard to claim 12, Havemann teaches in figures 5c and 5d; column 5, lines 49 – 67; and column 6, lines 15 – 25 wherein creating cavities is applying a vacuum to the substrate, dissolving the polymer.

It would further be obvious that Havemann applies to both the first and second disposable solids of Lur and Staudinger.

8. Claims 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of Abidi et al.

With regard to claim 13, Lur and Staudinger do not disclose an insulating layer deposited over the surface of the inductor. Abidi et al. teaches in figures 6a – 6c depositing an insulating layer (20) over the surface of an inductor (76) thereby encapsulating the inductor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the insulating layer of Abidi et al. to encapsulated the inductor of Lur and Staudinger in order to insulated the inductor from surroundings outside of the chip as is well known in the art.

With regard to claim 18, Lur and Staudinger do not specify properties of the inductor. Abidi et al. discloses in column 7, lines 34 – 37 an inductor having an inductance in excess of 1 nh and a self-resonance in excess of 10 MHz. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use an inductor with the disclosed properties of Abidi et al. in the method of Lur and Staudinger in order to have an RF tuned amplifier that can be fabricate having a large value monolithic inductor thereby substantially increasing as stated by Abidi et al in column 7, lines 35 – 42.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lur and Staudinger as applied to claim 1 above, and further in view of one of ordinary skill in the art.

It is not clear if the partially fabricated integrated circuit structure of Lur and Staudinger comprising transistors being CMOS and are interconnected to form an RF amplifier. It is well known in the art to form partially fabricated integrated circuit structures that are transistors being CMOS interconnected to form an RF amplifier. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use have the devices of Lur and Staudinger bet CMOS transistors in RF amplifier circuits in order to create a circuit that has exceptionally high input impedance (e.g. megohms), square law transfer characteristics which result in low cross modulation products, and wide dynamic operating range.

***Allowable Subject Matter***

10. Claims 3, 4 and 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination fails to disclose at least the step of creating two openings in an oxide layer located at opposite extremities of the oxide layer which is overlying a nitride layer used for the purpose of forming cavities. The openings located at

opposite extremities of the oxide layer have a diameter that is less than the dimension of the thickness of the oxide layer.

### ***Response to Arguments***

12. Applicant's arguments filed 7-30-01 have been fully considered but they are not persuasive.

13. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II  
January 7, 2003



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SUPERVISOR OF PATENT EXAMINER  
THURSDAY, JANUARY 9, 2003